Notice of Allowability	Application No.	Applicant(s)	
	09/735,256	BLOUIN ET AL.	
	Examiner	Art Unit	
	Freda A. Nelson	3628	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *After-Final Amendment and Telephone Interview of 8/22/07*.

2. ☒ The allowed claim(s) is/are *1-5, 7-12, 14-25, and 27*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☒ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

Response to Amendment

The amendment received on August 9, 2007 is acknowledged and entered. Claim 1 has been amended. Claims 6, 13 and 26 have been canceled. No claims have been added. Claims 1-5, 7-12, 14-25, and 27 are currently pending.

Claims rejections under 35 USC § 112 have been withdrawn due to the applicant's amendment.

The drawings filed on March 12, 2001 are accepted by the Examiner.

EXAMINER'S AMENDMENT

An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Pamela M. Riley (Reg. No. 40,146) on August 22, 2007.

The application has been amended as follows:

IN THE CLAIMS

1. (Currently Amended) A system for ~~predicting~~ calculating semiconductor product costs at a fabricator comprising:

a storage medium including a database of historical costs and historical critical gate dimensions of different technologies run at said fabricator;

a user interface adapted to receive user inputs for new design parameters and new critical gate dimensions associated with a new device to be produced at said fabricator; and a computer adapted to:

receive said user inputs; perform a regression analysis using said historical critical gate dimensions as independent variables and said historical costs as dependent variables, wherein said regression analysis produces relationship curves that only show relationships between said historical critical gate dimensions and said historical costs; and

~~predict~~ calculate product costs of said new device based on said user inputs and said relationship curves.

8. (Currently amended) A method of ~~predicting~~ calculating semiconductor product costs comprising:

storing, in a database, historical costs and historical critical gate dimensions of different technologies run at a fabricator;

performing a regression analysis using said historical critical gate dimensions as independent variables and said historical costs as dependent variables, wherein said regression analysis produces relationship curves that show only relationships between said historical critical gate dimensions and said historical costs;

inputting new design parameters and new critical gate dimensions of a new device into said database; and

~~predicting~~ calculating product costs of said new device based on said relationship curves.

15. (Previously Presented) A system for ~~predicting~~ calculating semiconductor product costs at a fabricator comprising:

a regression analyzer adapted to produce relationship curves that show relationships between historical critical gate dimensions and historical costs of different technologies run at said fabricator;

a user interface for inputting a new critical dimension of a new technology; and

a calculator for ~~predicting~~ calculating a cost of said new technology based only on said new critical gate dimension and said relationship curves.

21. (Currently amended) A computer program product stored a storage device readable by a computer, wherein said computer program product comprises a computer program for performing a method of ~~predicting~~ calculating semiconductor product costs, said method comprising:

storing, in a database, historical costs and historical critical gate dimensions of different technologies run at a fabricator;

performing a regression analysis using said historical critical gate dimensions as independent variables and said historical costs as dependent variables, wherein said regression analysis produces relationship curves that only show relationships between said historical critical gate dimensions and said historical costs;

inputting new design parameters and new critical gate dimensions of a new device into said database; and

~~predicting~~ calculating product costs of said new device based on said relationship curves.

Allowable Subject Matter

Claims 4-7, 11-12 and 16-17 are allowed.

The following is an examiner's statement of reasons for allowance:

1. As per independent claims 1, 8, 15, and 21, the best prior art, "21st Century Semiconductor Manufacturing Capabilities" (hereinafter referred to as "Manufacturing), in view of Evans et al. (Patent Number 6,775,647).

Farrell (US Patent Number 5,383,129) while disclosing a method of estimating cost of printing materials used to print a job on a printing apparatus, does not disclose or fairly teach:

perform a regression analysis using said historical critical gate dimensions as independent variables and said historical costs as dependent variables, wherein said regression analysis produces relationship curves that only show relationships between said historical critical gate dimensions and said historical costs; and

calculate product costs of said new device based on said user inputs and said relationship curves.

2. The best NPL prior art, "21st Century Semiconductor Manufacturing Capabilities" while disclosing Moore's Law and cost per chip goals, fails to disclose: a computer adapted to:

perform a regression analysis using said historical critical gate dimensions as independent variables and said historical costs as dependent variables, wherein said regression analysis produces relationship curves that only show relationships between said historical critical gate dimensions and said historical costs; and

calculate product costs of said new device based on said user inputs and said relationship curves.

3. The best foreign art, Yamada et al. JP 2000091178 while disclosing a production control method, fails to disclose a compter adapted to:

perform a regression analysis using said historical critical gate dimensions as independent variables and said historical costs as dependent variables, wherein said regression analysis produces relationship curves that only show relationships between said historical critical gate dimensions and said historical costs; and

calculate product costs of said new device based on said user inputs and said relationship curves

The remaining dependent claims are considered allowable, as they are dependent and based off of an allowable independent claim.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Freda A. Nelson whose telephone number is (571) 272-7076. The examiner can normally be reached on Monday - Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Hayes can be reached on 571-272-6708. The fax phone number for the organization where this application or proceeding is assigned is **571-273-8300.**

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

FAN 08/27/2007

JOHN W. HAYES
SUPERVISORY PATENT EXAMINER